## LECTURE 14 : PAGE TABLES

## Page Table Structure

■ Hierarchical Paging

- Hashed Page Tables
- Inverted Page Tables


## Hierarchical Page Tables

■ Break up the logical address space into multiple page tables.

- A simple technique is a two-level page table.


## Two-Level Paging Example

- A logical address (on 32-bit machine with 4 K page size) is divided into:
- a page number consisting of 20 bits.
- a page offset consisting of 12 bits.
- Since the page table is paged, the page number is further divided into:
- a 10-bit page number.
- a 10-bit page offset.
- Thus, a logical address is as follows:

| page number |  | page offset |
| :---: | :---: | :---: |
| $p_{\mathrm{i}}$ $p_{2}$ |  |  |
| $d$ |  |  |
| 10 | 10 | 12 |

where $p_{i}$ is an index into the outer page table, and $p_{2}$ is the displacement within the page of the outer page table.

## Two-Level Page-Table Scheme



## Address-Translation Scheme

- Address-translation scheme for a two-level 32-bit paging architecture



## Hashed Page Tables

- Common in address spaces > 32 bits.
- The virtual page number is hashed into a page table. This page table contains a chain of elements hashing to the same location.
- Virtual page numbers are compared in this chain searching for a match. If a match is found, the corresponding physical frame is extracted.


## Hashed Page Table



## Inverted Page Table

- One entry for each real page of memory.
- Entry consists of the virtual address of the page stored in that real memory location, with information about the process that owns that page.
- Decreases memory needed to store each page table, but increases time needed to search the table when a page reference occurs.
- Use hash table to limit the search to one - or at most a few - page-table entries.


## Inverted Page Table Architecture



